Remarks

Claims 143-155, 167-193 and 196-224 are pending.

Claims 1-142, 156-166, 194 and 195, which were restricted by the Examiner, have been canceled without prejudice to their future prosecution in one or more divisional applications.

The pending claims have been further amended to more clearly define Applicant's structures as comprising overlying layers of single crystal epitaxial silicon, each layer having a *faceted surface*. Support for the amendments is in the specification at page 2, lines 21-24 (emphasis added):

> ...The semiconductive substrate is exposed to a silicon comprising gas in an epitaxial (epi) growth chamber for a time and under conditions effective to form an epitaxial layer of monocrystalline silicon **having a faceted surface.**
>
> ...
>
> In a first step shown in FIG. 1B, with at least a portion of the oxide layer 28 having been removed to expose surface 14 of the monocrystalline silicon substrate 12, a first layer 34a of monocrystalline silicon is formed on the exposed surface by selective epitaxial growth. The first layer 34a comprises a single crystal 36a **that is preferably grown until a facet is formed on the top surface** 38a. The facet surface can be a (100), (110) or (111) plane orientation, with a (100) plane orientation preferred.
>
> ...
>
> **Once the facet is formed** on the top surface 38a of the crystal 36a, a thin insulative layer 42a is formed over the epitaxial layer 3...

No new matter has been added with the amendments, which are intended to merely clarify language used in the claims and the subject matter claimed. The scope of the claims is intended to be the same after the amendment as it was before the amendment.

Rejection of Claims under 35 U.S.C. §§ 102(b)/103(a)

At page 2, the Examiner rejected Claims 143-145, 147, 149-155, 167-193, and 196-202 under Section 102(b) as anticipated by USP 5,483,094 (Sharma). At page 5, the Examiner rejected Claims 146 and 148 as obvious over Sharma. At page 6, the Examiner rejected Claim 224 as obvious over Sharma in view of USP 5,849,077 (Kenney). These rejections are respectfully traversed.

As noted above, the claims have been amended to define Applicant's structures as comprising overlying layers of single crystal epitaxial silicon, each layer having a *faceted surface*.

The Examiner maintains that FIG. 12 of Sharma discloses at least two overlying crystals 33/34 of epitaxial silicon (citing to the Abstract, col. 3, line 42, and col. 8, line 5), with the "top surface of crystal 34 comprises a facet."

Sharma describes a memory cell made of an epitaxial silicon pillar (31), which has three different doped *regions* 32, 33, 34. Sharma dopes the lower and upper *regions* 32, 34 with an n-type dopant and the central region 33 with a p-type dopant, by incorporating the dopant using a gas into the silicon gas source.

Sharma does not describe forming individual epitaxial layers – *each layer* having a *faceted surface*. Nowhere does Sharma describe facet formation in the silicon pillar 31 as that term is known and understood in the art and/or how that term is used in Applicant's specification and the claims.

The Examiner is respectfully directed to the following references that describe and illustrate epitaxial silicon layers with "facets", which demonstrates how that term is known and used in the art:

1) **Ginsberg et al.**, "Selective epitaxial growth of silicon and some potential application," *IBM J. Res Develop.* 34(6): November 1990. **FIG. 1** (below) illustrates formation of a "facet" during epitaxial growth. See also the accompanying text below.

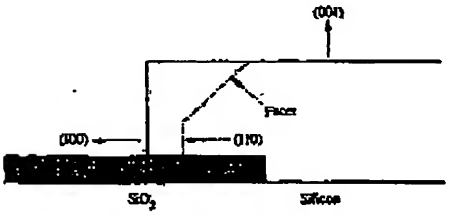
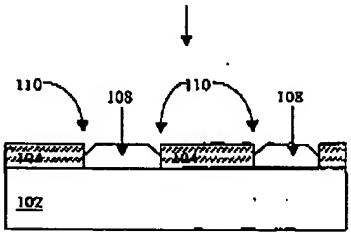


Figure 1

Epitaxial lateral overgrowth. Solid line represents overgrowth with crystallographically identical horizontal and vertical planes. Broken line represents growth along a <110> direction. Note formation of facet in the latter case.

3. Applications that are based on an extension of the SEG process, designated as the epitaxial lateral overgrowth (ELO) process, in which an opening in a dielectric layer can be used as a "seed" area for the selective growth of silicon. Growth occurs in the seeded area and is continued until it spreads laterally over the dielectric layer. If the edges of the insulation layer are oriented so that the horizontal and vertical planes are crystallographically identical, e.g., (100) horizontally and (001) vertically, equal growth rates can result for both directions. This is depicted in Figure 1 for an oxidized silicon wafer containing an opening in its oxide layer. (Although it is also possible for facets to form as the result of differing growth rates for other crystallographic planes, such as the {111} planes [26], their formation can be minimized by varying deposition conditions.) If the overgrowth is continued for a sufficient time, it is possible for the epitaxial silicon

2) **USSN 20040175893** (Apparatuses and methods for forming a substantially facet-free epitaxial film) at paragraph [0006], describes prior art processes with reference to FIG. 1. As stated below (emphasis added): "faceting is the formation of another growth plane at a different angle from the major surface of the epitaxial silicon regions..."



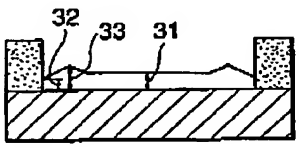
[0006] Selective deposition methods used to form epitaxial film, such as the epitaxial silicon, *typically causes faceting. As illustrated in FIG. 1, each of the epitaxial silicon regions 108 contains facets 110.* Faceting is the formation of another growth plane at a different angle from the major surface of the epitaxial silicon regions and often, at the sides of the regions that meet the wall of the structures already formed on the substrate. For example, the facets 110 on the epitaxial silicon regions 108 are formed at the sides that meet the wall of the silicon oxide film 104.

3) **USP 6,074,478** (Method of Facet Free Selective Silicon Epitaxy) at col. 1, lines 28-43 (emphasis added) and FIG. 3(a):

Now, in conventional selective epitaxy, regions of small film thickness where crystal planes with certain orientations, called *facets, tend to be formed in the end parts* (parts where the grown film makes contact with an insulating film) *of the grown film*. When these facets are formed, the depth of a diffused layer under such a facet region becomes large, making it difficult to form a shallow junction.

The cause of the formation of a facet is the difference in the surface energy which depends on the orientation of the crystal plane. The surface energy of silicon differs with the orientation of the crystal plane, for example, the (100) plane has a surface energy higher than those of the (111) plane and the (311) plane. *Accordingly, on the silicon substrate of the (100) plane. epitaxial growth proceeds with the formation not only of the (100) plane but also of the (111) and (311) planes that have lower surface energies.*

FIG.3(a)



The film thickness 31 at the central part of the epitaxial film, the film thickness 32 at the extreme end parts (parts where the film makes contact with the silicon oxide film), and the maximum film thickness 33, as shown in FIGS. 3(a) and 3(b), are measured to evaluate the extent of occurrence of the facets and the loading effect. Here, *FIGS. 3(a)* and 3(b) are the schematic diagrams of the cross sections of the epitaxial film for the cases *with* and without, respectively, ***the formation of the facets***.

Next, the evaluation result of the epitaxial film based on the first embodiment and the reference example 1 will be described. In the case of the reference example 1, ***facets are formed giving a film structure as illustrated in FIG. 3(a).*** In contrast, in the first embodiment, a film with extremely flat structure is formed with no facet formation, and an increase in the film thickness at the end parts of the epitaxial film, as shown in FIG. 3(a), does not take place.

A facet – as that term is known and used in the art, means a growth plane or crystal plane formed at various angles or orientations. As illustrated above, a facet is an angled face that forms as the result of differing growth rates for other crystallography planes.

The Examiner is further directed to Applicant's description of forming an epitaxial silicon layer having "a faceted surface" (specification at pages 4-5, bridging paragraph), and the description of forming a facet on the top surface of the epitaxial silicon layer (page 9, lines 14-16) (emphasis added):

In one embodiment of the method of the invention, a vertical structure can be formed on a semiconductive substrate. The method involves selectively growing a first epitaxial layer of monocrystalline silicon on the surface of the substrate. Prior to the SEG step, it is desirable to remove oxide from the area on the substrate where the structure is to be formed, for example, by a dry oxide etch. The semiconductive substrate is exposed to a silicon comprising gas in an epitaxial (epi) growth chamber *for a time and under conditions effective to form an epitaxial layer of monocrystalline silicon having a faceted surface*. The epitaxial layer comprises a single silicon crystal having vertically oriented sidewalls and a top horizontal surface, preferably defining a facet having a (100) plane orientation.

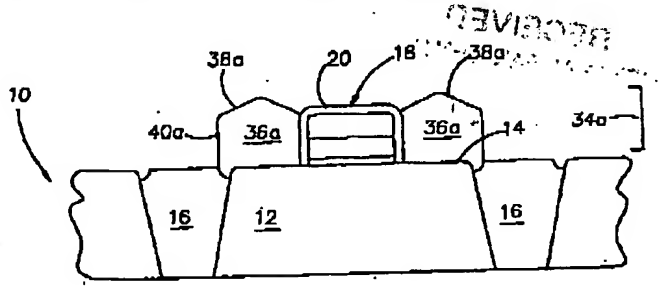


FIG.1B

In a first step shown in FIG. 1B, with at least a portion of the oxide layer 28 having been removed to expose surface 14 of the monocrystalline silicon substrate 12, a first layer 34a of monocrystalline silicon is formed on the exposed surface by selective epitaxial growth. The

first layer 34a comprises *a single crystal 36a that is preferably grown until a facet is formed on the top surface 38a. The facet surface can be a (100), (110) or (111) plane orientation, with a (100) plane orientation preferred.* The plane orientation can be determined by known techniques in the art, for example, by cross-section and measuring the angles between the substrate and epi film, for example by scanning electron microscope (SEM) or transmission electron microscope (TEM).

As taught by Applicant in the specification[1] and illustrated in the Figures, each layer of epitaxial silicon is individually grown until *a faceted surface* is formed.

The claims as amended clarify that each individual layer of epitaxial silicon has a faceted surface. Sharma does not teach or suggest such a structure.

Sharma describes the formation of the silicon pillar 31 with doped regions 32, 33, 34 at col. 3, line 42 to col. 4, line 27 (emphasis added). This process is illustrated in FIGS.2-3 below.

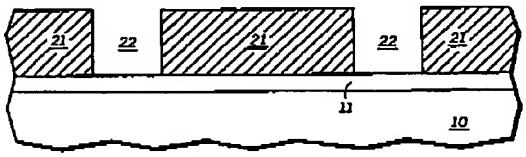


FIG.2

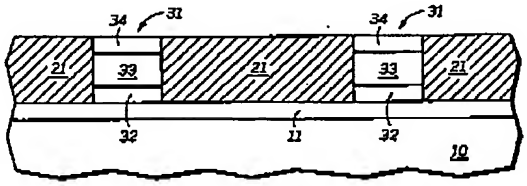


FIG.3

A first insulating layer 21 is formed over the buried layer 11 and patterned to include openings 22 as shown in FIG. 2. The thickness of the first insulating layer should be about at thick as subsequently formed silicon pillars. In this embodiment, the first insulating layer is about 8000 angstroms thick.

Silicon pillars 31 are selectively and epitaxially grown from exposed portions of the buried layer 11 lying at the bottoms of the openings 22 as shown in FIG. 3. Each silicon pillar 31 includes a lower doped region 32 that acts as part of the source region for the memory cell, a central region 33 that acts as the channel region for the memory cell, and an upper doped region 34 that acts as the drain region for the memory cell. The regions 32 and 34 are n-type doped, and the central region 33 is p-type doped...

In this embodiment, the silicon pillars 31 are formed using a conventional method. The formation may be performed by low pressure chemical vapor deposition using a silicon hydride (silane, disilane, or the like), a silicon-chlorine compound (dichlorosilane or the like),

[1] Also see the title of the application: "...Controlled Selective Epitaxial *Growth of a Facet*..."

> or a combination thereof. The temperature of the epitaxial growth depend in part on the gaseous silicon source. For example, if dichlorosilane is used, the temperature may be between 750-900 degrees Celsius. In general, the temperature of the epitaxial growth increases as the relative ratio of chlorine atoms to silicon atoms increases within the molecule of the silicon source gas. The lower and upper doped regions 32 and 34 are doped with an n-type dopant. The n-type dopant may be incorporated by using a gas containing an n-type dopant, such as phosphine, arsine, and the like. The central regions 33 are doped with a p-type dopant. The p-type dopant may be incorporated by using a gas containing p-type dopant, such as diborane, boron trichloride, and the like. The doping levels within regions 32-34 are determined in part by the relative flow rate between the silicon source and the dopant gas. One skilled in the art can adjust the relative gas flow rates to obtain the desired doping concentrations.

Sharma does not describe forming individual epitaxial layers – *each layer* having a *faceted surface*. Nowhere does Sharma describe facet formation in the silicon pillar 31 as that term is known and understood in the art and/or according to Applicant's disclosure.

Sharma does not describe a process whereby each region 32, 33, 34 is separately grown *until a faceted surface forms* – as with Applicant's structure.

In Applicant's device, each layer of epitaxial silicon is grown until a faceted surface is produced – whereupon a dielectric layer is deposited, and the dielectric layer is etched to expose the surface of the underlying epitaxial layer. Another epitaxial layer is then grown until a faceted surface is produced. Thus, Applicant's structure is a series of overlying faceted layers of epitaxial silicon – each layer being grown until a faceted surface has been formed.

Applicant believes that the claims as amended clearly define over the cited prior art.

As for the rejection of Claim 224, the added disclosure of Kenney does not make up for the deficiencies of Sharma's disclosure.

Sharma's disclosure of an epitaxial silicon pillar containing doped regions does not teach or suggest Applicant's structures as claimed. Accordingly, withdrawal of these rejections is respectfully requested.

Rejection of Claims under 35 U.S.C. §§ 102(b)/103(a)

The Examiner rejected Claims 203-223 under Section 102(b) as anticipated by or obvious over USP 5,483,094 (Sharma). This rejection is respectfully traversed.

As noted above, the claims have been amended to define Applicant's structures as comprising overlying layers of single crystal epitaxial silicon, each layer having a *faceted surface*.

The Examiner maintains that the process limitations in Claims 203-223 "do not carry weight in a claim drawn to structure," citing to *In re Thorpe*, 277 USPQ 964 (Fed. Cir. 1985).

It is well established that product claims may include process steps to wholly or partially define the claimed product. *In re Brown*, 173 USPQ 685, 688 (1972), and the cases cited therein. *To the extent these process limitations distinguish the product over the prior art, they must be given the same consideration as traditional product characteristics.* *In re Luck*, 177 USPQ 523, 525 (CCPA 1973); *In re Hallman*, 210 USPQ 609, 611 (CCPA 1981).

These claims recite the following steps:

– selectively growing a first faceted epitaxial silicon layer on a substrate;

– depositing an insulative layer over the first epitaxial layer;

-- removing a portion of the insulative layer to expose the surface of the first epitaxial layer;

– selectively growing a second faceted epitaxial silicon layer on the first epitaxial layer;

-- depositing an insulative layer over the epitaxial layers.

The foregoing process limitations distinguish Applicant's product over the prior art – and must be give consideration by the Examiner.

First of all, the resulting structure is distinguished from Sharma by the formation of two overlying *faceted* epitaxial layers. Nowhere does Sharma describe such a formation.

Second, unlike Sharma, Applicant does not grow the gate structure *within an opening* in an insulative layer. Rather, Applicant selectively grows successive overlying and faceted epitaxial layers on a substrate – without the benefit of a confined space such as an opening in an insulative layer as taught by Sharma.

This poses a problem because crystal growth by SEG along a select facet of a single-crystal silicon layer to form a vertically oriented structure cannot be controlled by varying the growth conditions due to the existence of facets on the crystal having different orientations (i.e., (100), (110), (111)). However, such control is needed to achieve vertically oriented epitaxial growth and eliminate lateral or horizontal growth that can short circuit closely positioned adjacent devices.

To achieve this, after growing each faceted epitaxial layer — *an insulative layer* is deposited over the sidewalls of the epitaxial layer. This *eliminates* unwanted lateral growth of a subsequent epitaxial layer from a lateral facet of the underlying epitaxial layer, resulting in an upright structure.

The steps of depositing an insulative layer after the growth of each epitaxial layer further distinguishes Applicant's structures from Sharma.

For example, in a structure having two overlying faceted epitaxial layers, a first epitaxial layer is grown and a first insulative layer is deposited over that layer. Then, a second epitaxial layer is grown and a second insulative layer is deposited over both of the first and second epitaxial layers. As a result, the second (upper) epitaxial layer is covered by a single thickness of an insulative layer — compared to the first (lower) epitaxial layer, which is covered by *two* thicknesses of an insulative layer

By comparison, Sharma does not deposit any insulative material onto the pillar (31). Rather, as shown in FIG. 2 above, Sharma forms a pillar *within an opening (22)* etched into an insulating layer. This does not result in Applicant's structure as claimed.

The structural characteristics resulting from the claimed process steps clearly distinguish Applicant's devices and structures as recited in Claims 203-223 from Sharma's silicon pillars (31).

Sharma's disclosure of an epitaxial silicon pillar containing doped regions does not teach or suggest Applicant's structures as claimed. Accordingly, withdrawal of this rejection is respectfully requested.

Information Disclosure Statement. Applicant brings to the Examiner's attention the enclosed Form 1449/PTO. Applicant respectfully requests that these references be made of record in the present application, and that an initialed copy of the Form 1449/PTO indicating consideration of these references by the Examiner be returned to Applicant in the next communication.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that a two (2) month extension of term is required. Please charge the required fee to Account No. 23-2053. If an additional extension is required, please consider this a petition therefor, and charge the required fee to Account No. 23-2053.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine M Strodthoff

Dated: August 8, 2005

Kristine M. Strodthoff
Reg. No. 34,259

WHYTE HIRSCHBOECK DUDEK S.C.
555 East Wells Street
Suite 1900
Milwaukee, Wisconsin 53202-3819
(414) 273-2100

Customer No. 31870

Appendix

Form 1449/PTO